RMAP – software for resistance verification of power nets and ESD protection structures

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Biography

Maxim Ershov received M.Sc. degree from Moscow Institute of Physics and Technology, and Ph.D. degree from Russian Academy of Sciences, in solid state electronics. His research interests are in the areas of semiconductor device and interconnects physics, numerical simulation, and parasitic extraction. In Silicon Frontline Technology, Maxim is leading the research, development, and applications of software tools for parasitic capacitance and resistance extraction, simulation, and analysis of large area electronic devices and systems, including power devices and ESD devices and networks.

Abstract

This paper presents RMAP - a new software tool and methodology for electrical verification of power nets and ESD protection structures. RMAP calculates resistances from the pads to all points on a net, and presents the results as color maps, enabling quick interactive visual inspection. Layout errors – narrow long metal lines, missing or insufficient number of vias, poorly connected pads, etc. – are immediately seen on the resistance plots, even for un-zoomed full chip view. Verification time is reduced by orders of magnitude as compared to visual inspection of layout views, and to IR voltage drop tools. Typical applications of RMAP include catching layout errors, verifying resistance to ESD devices and guard rings, analyzing common resistance problems, where resistance can be used as a proxy for problems related to IR voltage drop during normal circuit operation or under stress conditions (ESD, latchup, etc.).

Introduction

- **Electrical verification of power nets is a complex task**

- **Existing approaches:**
  - ☐ Visual inspection of large size printouts of power nets (1x1 meter)
  - ☐ Use of complex IR drop and EM analysis tools
  - ☐ Tedious, time consuming, error prone, require expert user

- **Layout errors often manifest themselves as high resistance**

- **A need in a tool for quick identification of the layout errors:**
  - ☐ Easy to set up, use, and analyze results – by a non-expert
  - ☐ Usable at all design stages (from early on to final stages)
  - ☐ Fast and efficient

Basic functionality of Rmap

- Automated calculation of resistance from pad(s) to each point of a net (all metal layers), minimum input from the user

- Presenting results as color maps, for interactive analysis

- Quick visual identification of layout problems

- Simple setup: define pads → get Rmap plots → immediately see problems, highlighted by color

- Convenient interactive environment for layout problem debugging
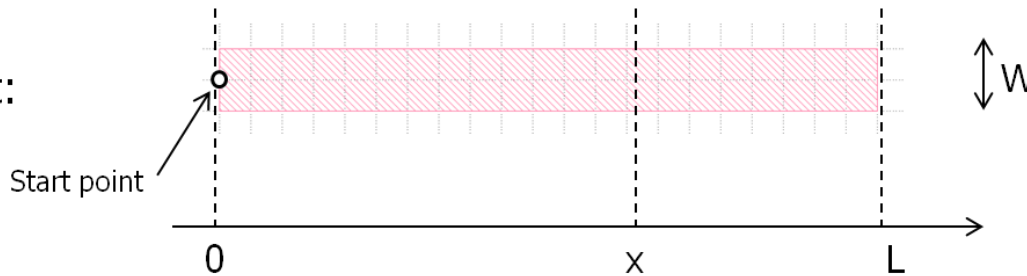
- Can be used at early design stage or for the final sign-off verification

The concept of resistance mapping
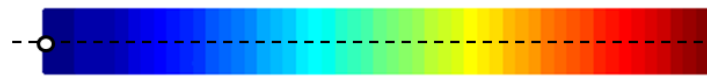
RMAP of straight metal line

Layout:

Start point

0 x L

W

Analytical model:

$$R = \rho \frac{x}{W}$$
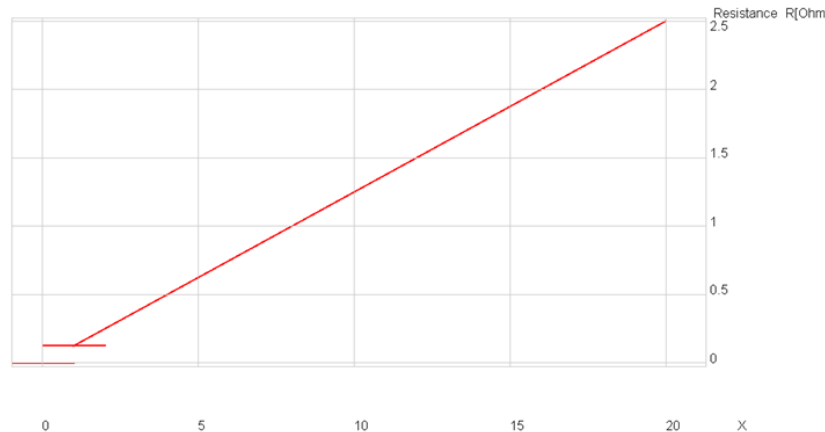
Rmap plot:

Resistance R[Ohm]
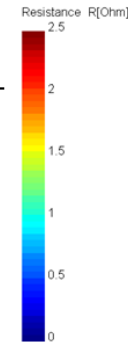
Cut line (1D plot):

Resistance R[Ohm]

■ Rmap shows resistance from starting point(s) to every point on a line (net) as a color map

Advantages of Rmap tool

- Fully automated simulation flow, minimum input from user

- Ease of setup and use

- Layout errors pop up as red color or color gradient

- Can be used by any designer and engineer

- Can be used early in the design stages and for final sign-off

- Synchronization of Rmap view with layout editor view

Layout errors identified by Rmap

- Too narrow and long metal lines

- Missing or insufficient number of vias

- Poor connection of pads to power nets

- High resistance from pads to ESD devices

- Electrical connectivity through high-resistive layers

- Color effects revealing potential problems
  - High resistances seen as "hot spot", shown by red color
  - Abrupt color changes
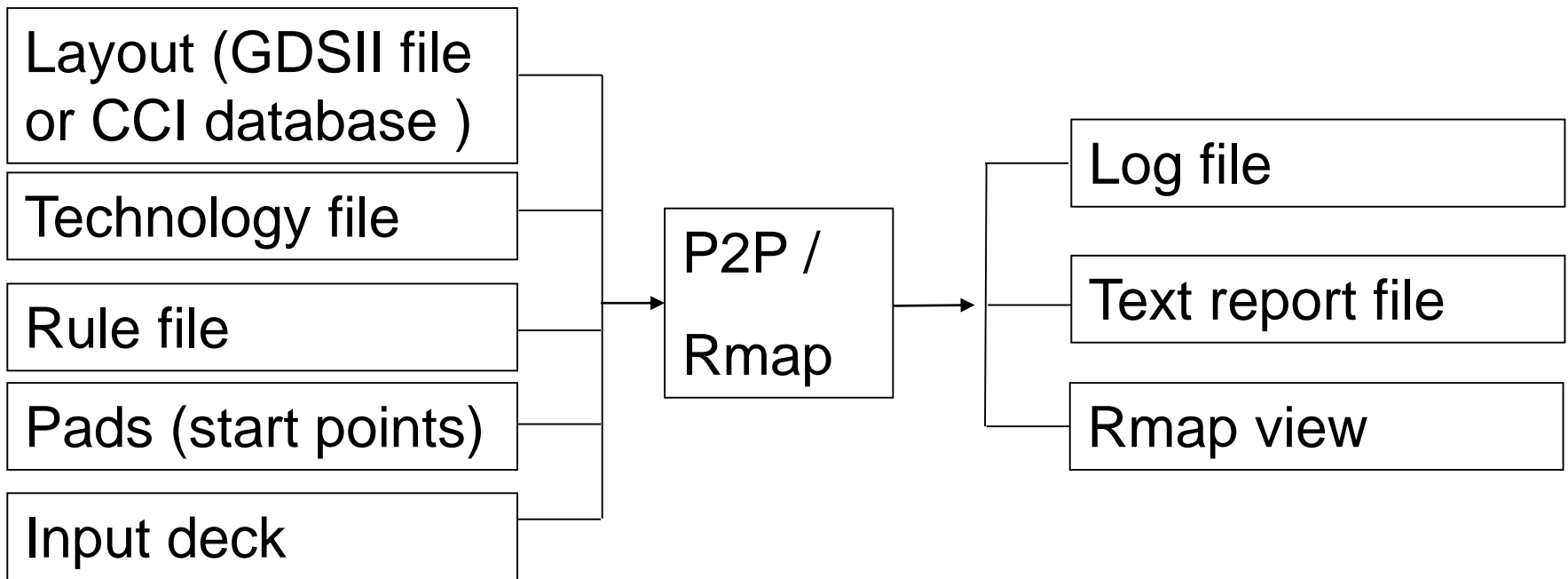 - Different colors crossing (i.e. missed vias)
  - Continuous rainbow-like color gradients – path to high R areas

Typical applications

- Resistance from pads to various blocks for ground / power nets (or any nets)

- Resistance to ESD devices and guard rings

- Common resistance problem for several ground nets connected at the pad

- Guard ring resistance verification

- Verification of IP blocks and their integration into full chip

Rmap usage model

- Run Rmap simulation
  - From minute to hours, depending on design and resolution
- Review text reports for high resistance
- Visualize resistance maps with GUI tool (R3DDRAW)
  - Identify high resistance areas
  - Trace color gradients to understand the root causes
  - Optionally, run P2P for current density analysis
- Fix layout errors
- Repeat these steps until problems are fixed
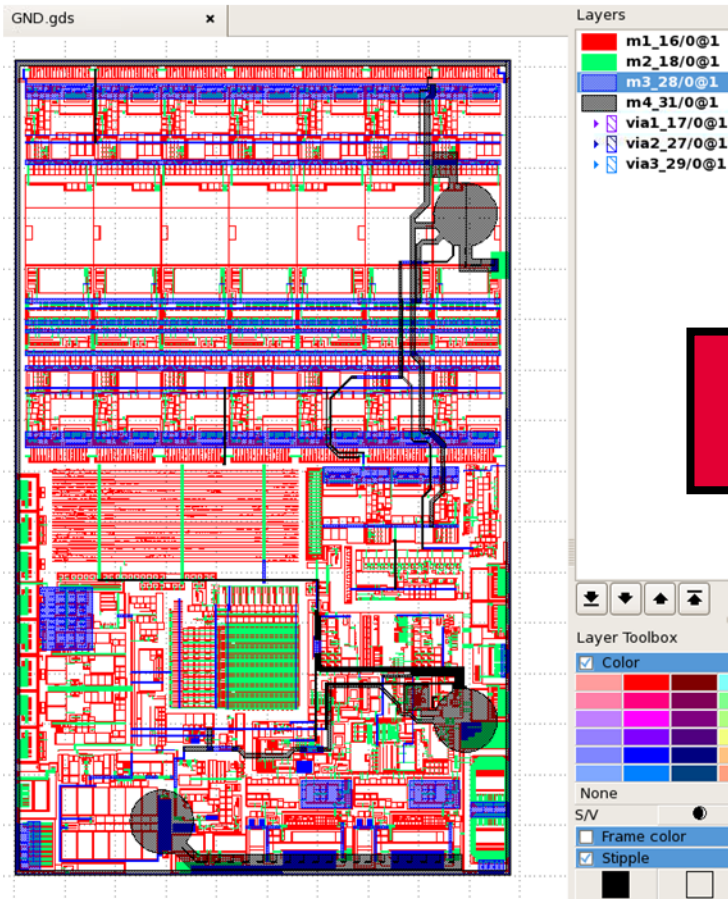- Faster and better quality layouts from layout teams
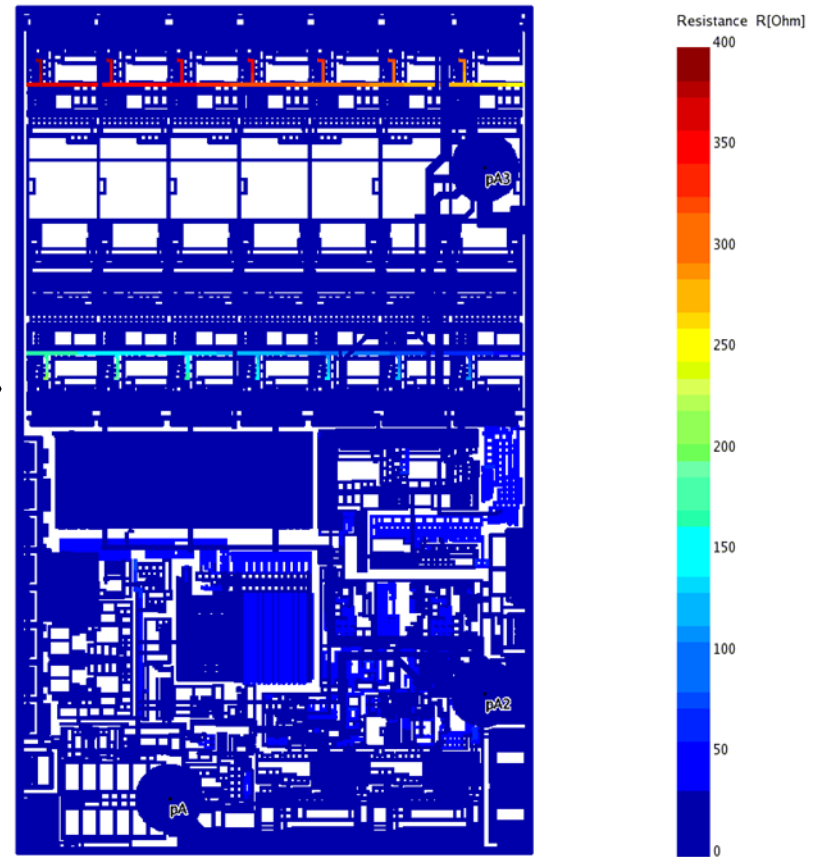
Rmap simulation flow

Layout (GDSII file or CCI database)
Technology file
Rule file
Pads (start points)
Input deck

→ P2P / Rmap →

Log file
Text report file
Rmap view

- ■ Rmap is one of functionalities of P2P tool
- ■ Geometry processing, R extraction, simulation
  - ☐ Fully automated

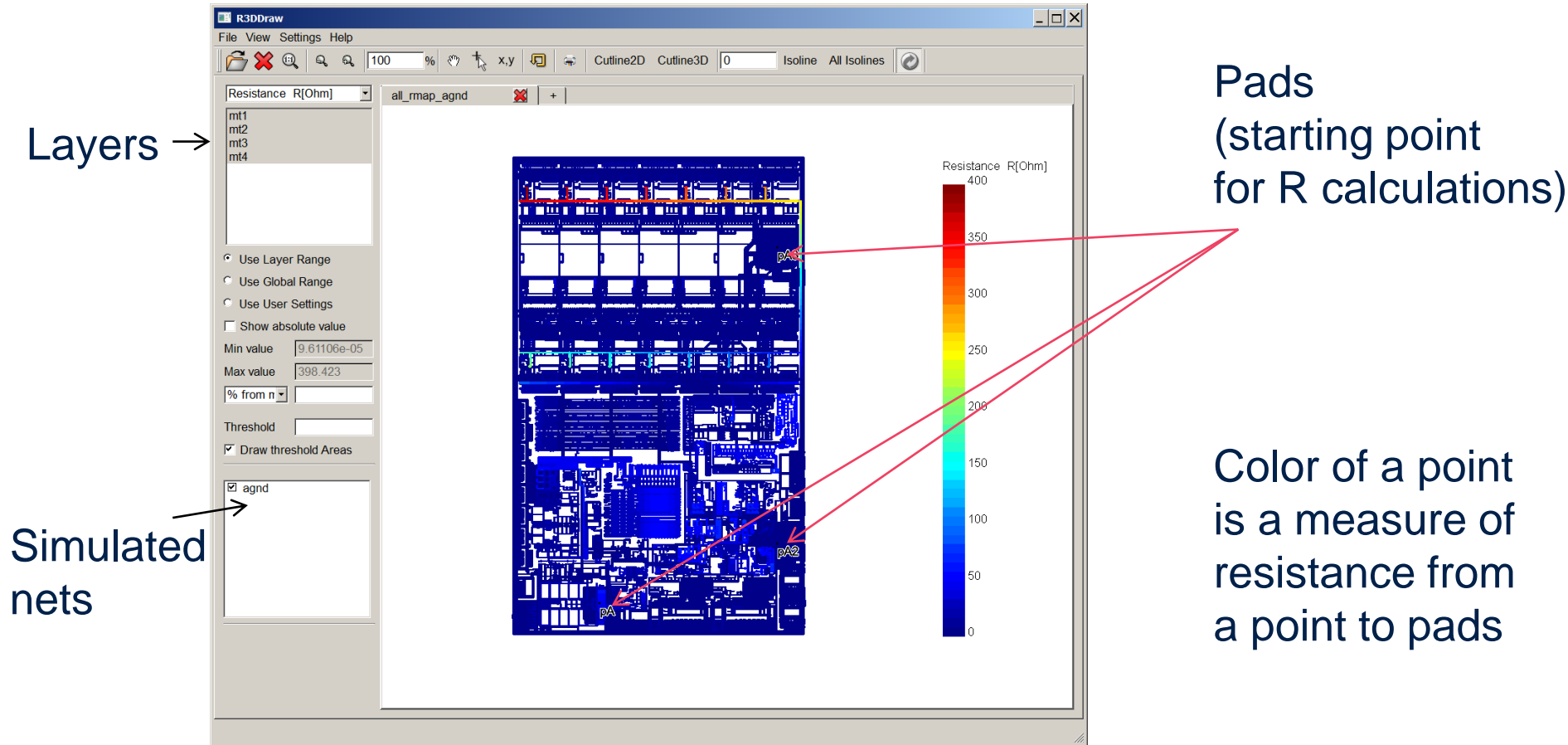# Resistance map analysis

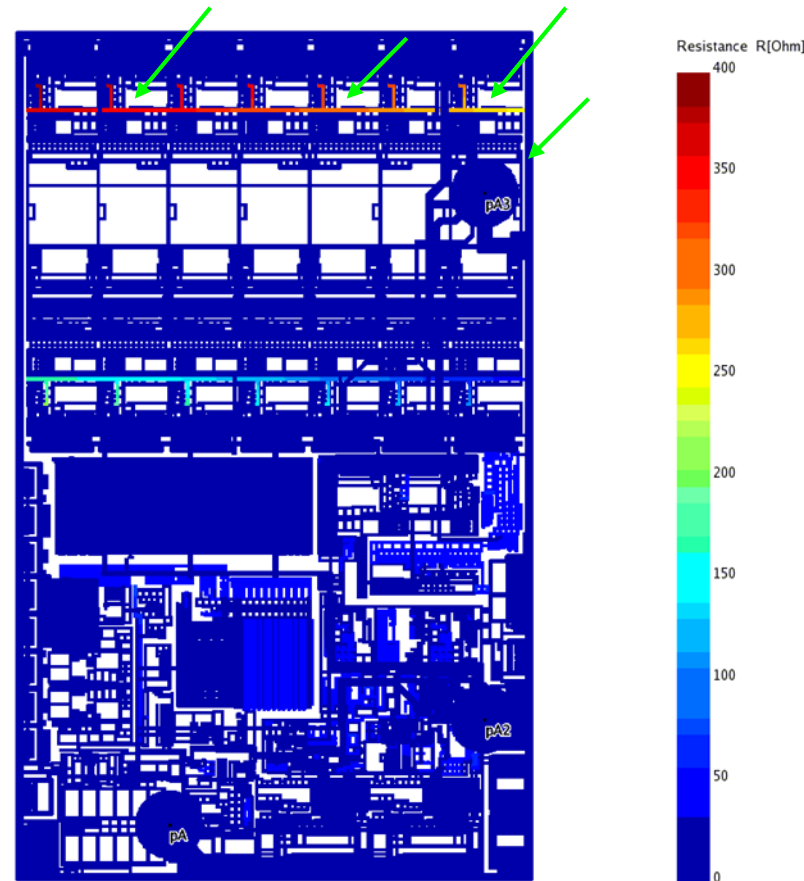

Layout

Rmap plot (all layers)

■ Hard to analyze

■ Easy to analyze

Vsiualizing Rmap results – R3DDRAW

Layers →

Simulated nets

Pads
(starting point
for R calculations)

Color of a point
is a measure of
resistance from
a point to pads

- Rmap results are visualized using a GUI-based tool
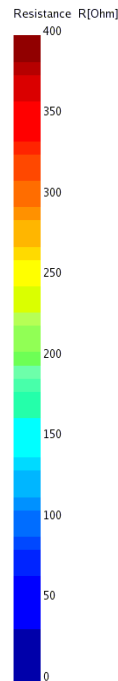
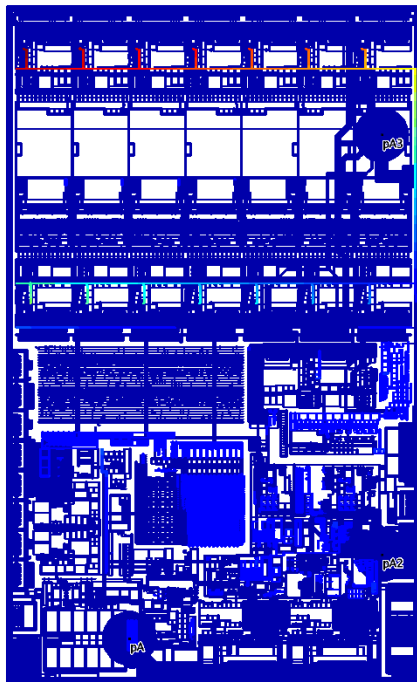- R3DDRAW enables an interactive analysis of Rmap results

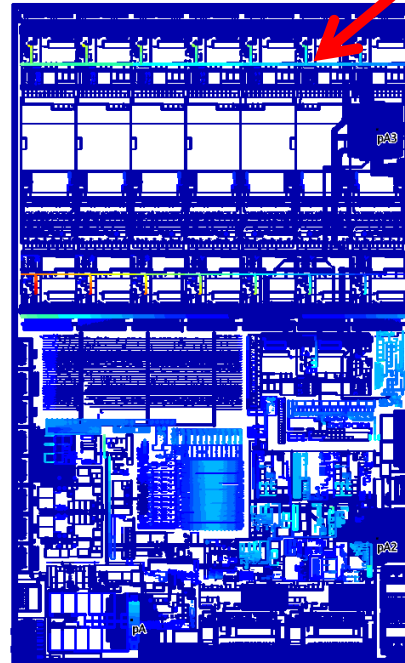# Tracing resistance paths

■ Tracing resistance color gradient reveals root causes

☐ In this case – very long narrow M3 line

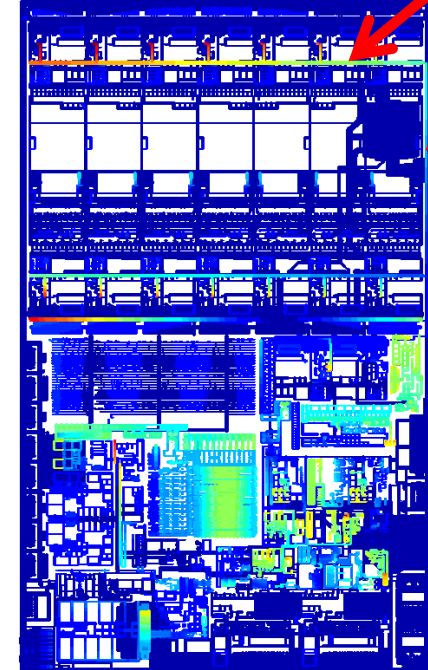# Layout improvement process
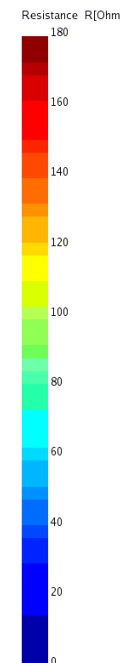
Original
$R_{max}=400$ Ohm

Improvement 1
$R_{max}=180$ Ohm

Improvement 2
$R_{max}=100$ Ohm

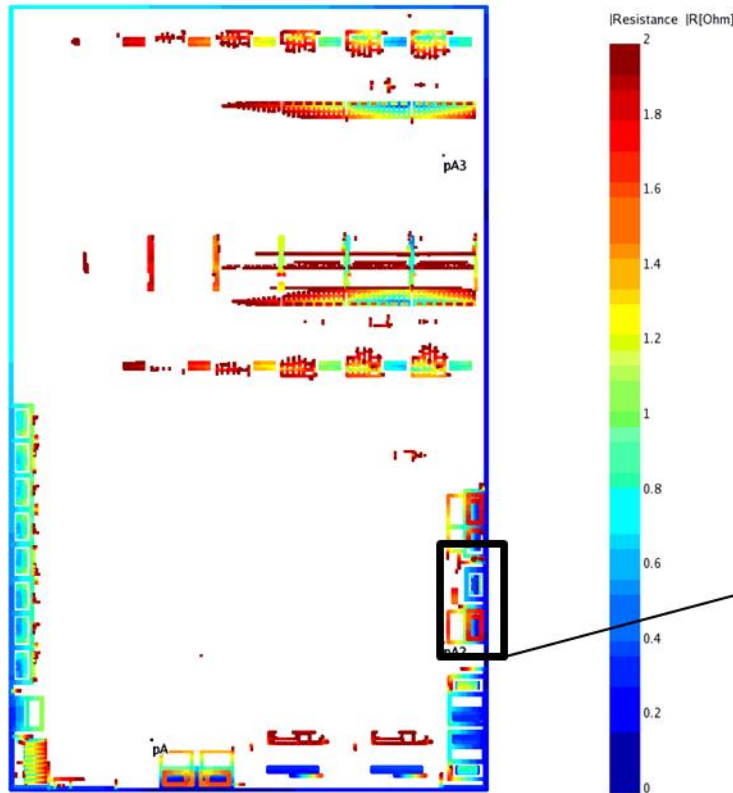Horizontal M3 line widened
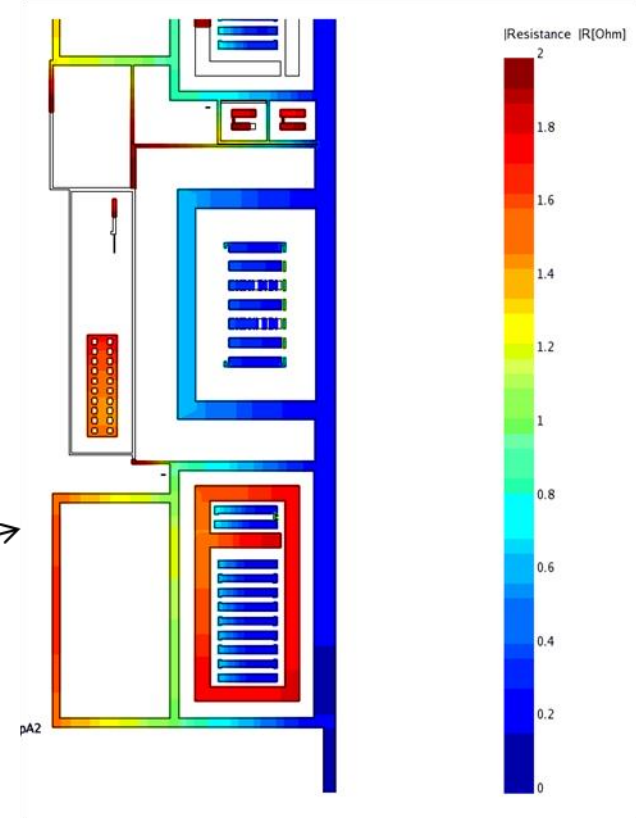
Horizontal and vertical
M3 lines widened

- Rmap enables a quick optimization and improvement process

ESD device and guard ring verification
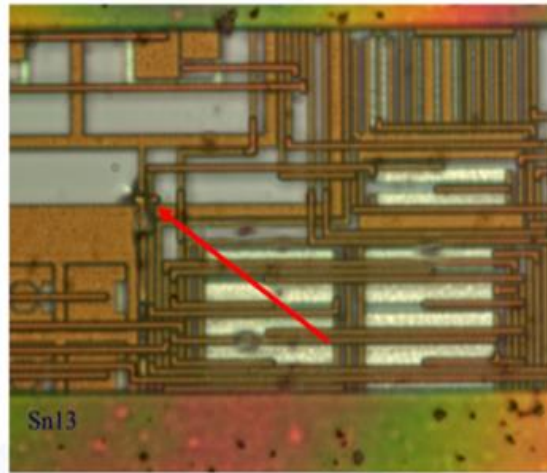

M1 resistance (below 2 Ohm)

Zoomed in view
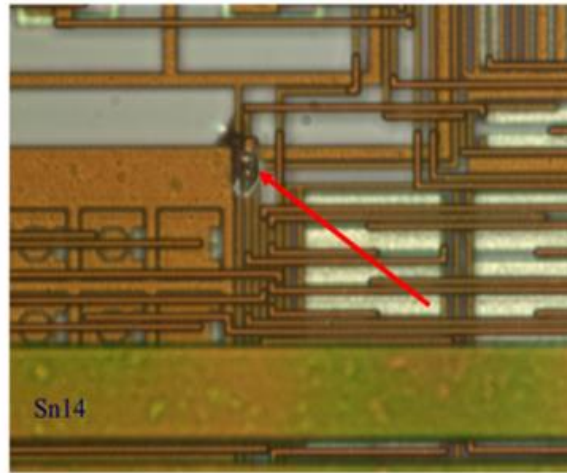
◆ Changing resistance range enables quick resistance verification of ESD structures, guard rings, and other blocks
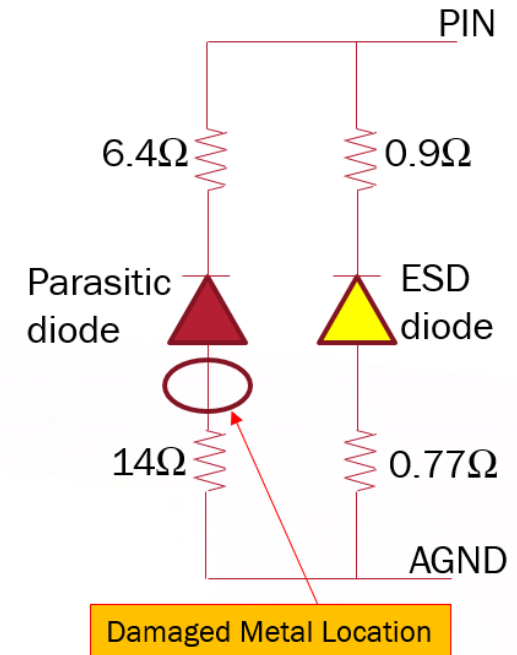
Pad to ESD device resistance – FA data

1500V HBM

2000V HBM

- ■ Chip was failing negative HBM stress on one pad
- ■ Failure Analysis results:
  - ☐ Parasitic diode AGND to PIN is carrying current during ESD zap
  - ☐ Metal line connected to AGND is damaged during ESD zap

Pad to ESD device resistance

Original layout (failed ESD test)
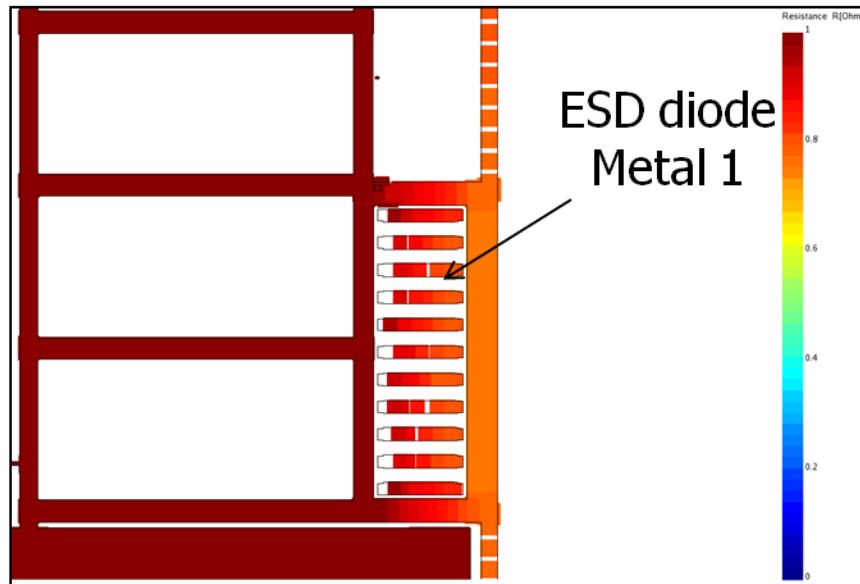
ESD diode Metal 1

Average resistance: ~0.8 Ohm

Fixed layout (passed ESD test)

Reduced resistance
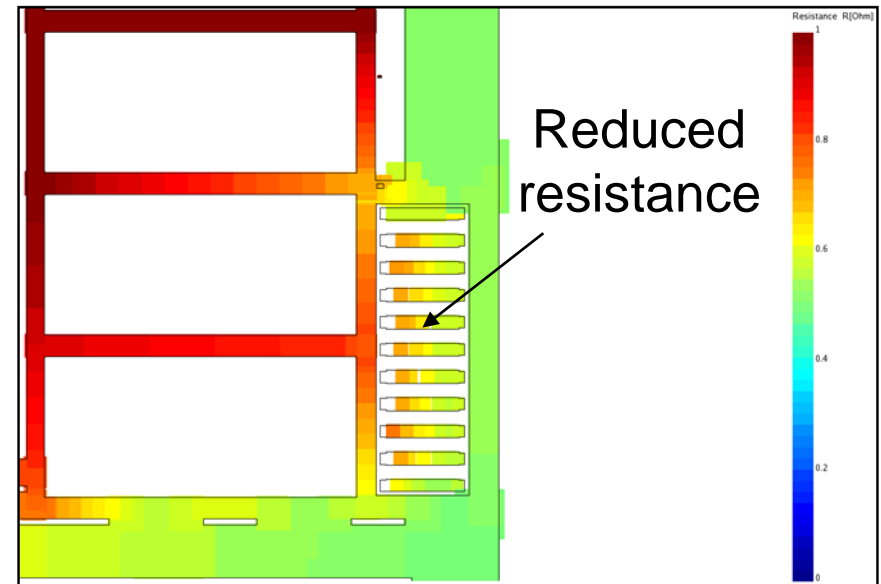
Average resistance: < 0.5 Ohm

- Rmap showed high resistance from pad to ESD diode fingers
- Improved metallization reduced resistance to below 0.5 Ohm
- Chip passed HBM test

Rmap features

- **Several functionalities in one tool:**
  - ☐ Geometry processing, R extraction, identification of points to be simulated, R simulation, visualization

- **Minimalistic input**
  - ☐ Design-specific: pads locations, GDSII layout
  - ☐ Pads are defined in input deck or extracted from GDS file
  - ☐ Technology-specific: tech file, rule file

- **Fast, easy to learn and use, applicable at early design stages**

- **GUI-based visualization is a very important part of Rmap**

- **Rmap offers a unique functionality not present in other tools**
  - ☐ See next slide for tool comparison

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Rmap comparison with other tools

Functonality	P2P / Rmap	Other tools
Port-to-port resistance calculation	Yes	Yes
DC IR / EM analysis	Yes	Yes
Transient IR drop analysis	No	Yes
Rmap plots	Yes	No
Easy to set up and use	Yes	No
Can be used by layout engineers	Yes	No
Requires LVS-clean design	No	Yes
Multiple functionalities "under one hood" (extraction, simulation, visualization)	Yes	Yes / No

Rmap limitations

- Rmap captures problems that are revealed by resistance color

- Problems that may be missed by Rmap

  - Current density hot spots not leading to high resistance

  - Short narrow segments in metal lines (see next slide)

  - One via instead of via array – small R, but high current density

- Rmap may highlight areas with no problems

  - Rmap does not take into account current flow in circuit operation

  - Zero / small current high resistance lines (e.g. sense line)

- Rmap uses 1D resistance extraction → 2D current crowding effects missed

Rmap versus current density plots

Layout	Rmap [Ohm]	Current density (P2P) [A/um]
A		
B		
C		
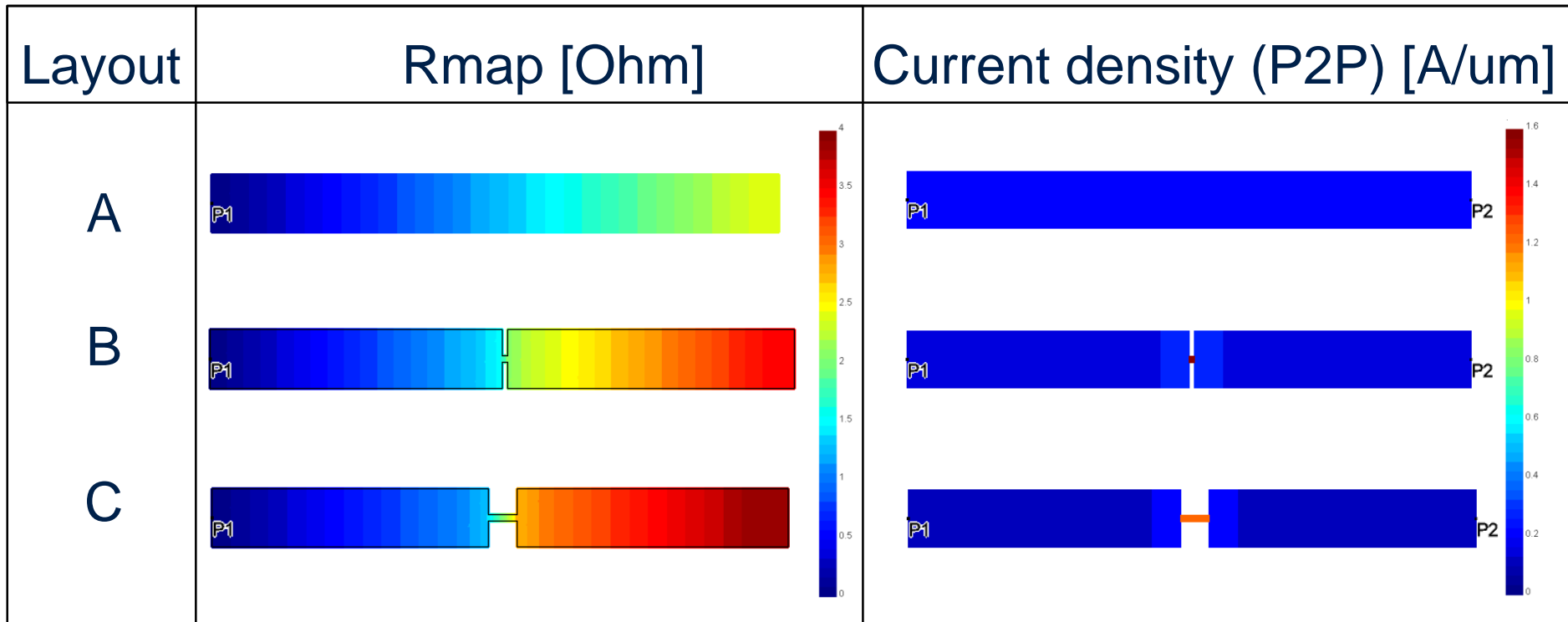
- ■ Current density hot spots may not reveal themselves in Rmap
  - ☐ Layout B - short narrowing – no abrupt color change in Rmap
  - ☐ Layout C – longer narrowing shows up as color discontinuity
- ■ Current flow / P2P simulations capture current density issues

Conclusions

- Rmap – a new software tool for of power nets verification is presented

- Rmap enables quick visual approach for power net analysis

- Resistances from pads to each point on power net are calculated and presented as color plots, over the layout

- Majority of layout problems can be identified and fixed quickly

- Remaining problems can be captured with IR / EM analysis provided by P2P tool

- Rmap can be used early in the design stages

- Minimalistic and simple input makes tool attractive for layout engineers, and for infrequent and novice users

References

- ESDA report: ESD TR18.0.01-14 – ESD Electronic Design Automation Checks

  - http://www.esda.org/Documents.html

- M. Ershov, Y. Feinberg, M. Cadjan, D. Klein, and M. Etherton, "EDA software for verification of metal interconnects in ESD protection networks at chip, block, and cell level", ESD Symposium Proc., 2013.

- http://www.siliconfrontline.com/products/p2p